DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a display device, and more particularly to a method for arranging a plurality of transistors which are prepared by a pseudo single crystallization technique (SELAX: Selectively Enlarging LAser X'tallization or a method similar to this SELAX) (for example, pair transistors).

A TFT (Thin Film Transistor) type liquid crystal display module has been popularly used as a display device of a notebook type personal computer or the like.

As the liquid crystal display module, there has been also known a display module which forms thin film transistors (TFT) on polysilicon.

On the other hand, a technique which recystallizes polysilicon or amorphous silicon in the lateral direction (direction parallel to a substrate) using laser beams so as to increase a particle size thereof (see brochure of International Publication 97/45827 (hereinafter referred to as a patent literature 1) and Society for Information Display 2002 (SID 02) DIGEST pp. 158-161 (hereinafter referred to as a non-patent literature 1)).

For example, it has been reported that by forming thin film transistors on a semiconductor (silicon) layer which is

formed by a method described in the above-mentioned non-patent literature 1, the mobility (μ) can be enhanced about three times compared to thin film transistors formed on a usual polysilicon film.

SUMMARY OF THE INVENTION

Fig. 11 is a view for explaining a pseudo single crystallization method of polycrystalline silicon using laser beams described in the above-mentioned non-patent literature 1.

In this method, laser beams 4 are irradiated to a polycrystalline silicon film 2 formed on a glass substrate 1 while scanning the glass substrate 1 in the direction of an arrow A shown in Fig. 11. As the laser beams 4, continuous (CW: Continuous Wave) laser beams are used.

Due to this laser beam irradiation, a temperature of the polycrystalline silicon film 2 is elevated and hence, the polycrystalline silicon film 2 is melted. Then, when the irradiation position advances to the next position, the temperature of the polycrystalline silicon film 2 is again lowered so that the polycrystalline silicon film 2 is recrystallized whereby a polycrystalline film which has particles thereof large-sized in a thin strip shape in the lateral direction is formed.

Hereinafter, in this specification, this polycrystalline

film is defined as a pseudo single crystal region 3. However, the method for forming the pseudo single crystal region 3 is not limited to the method described in the non-patent literature 1 and the polycrystalline film formed by a method similar to the method described in the non-patent literature 1 is also included in the definition of the pseudo single crystal region 3.

Since such melting and recrystallization advance in the direction opposite to the scanning direction (the direction of the arrow A shown in Fig. 11) of the glass substrate 1, the crystal growth direction (the direction of an arrow B shown in Fig. 11) of the pseudo single crystal region 3 assumes the direction parallel to and opposite to the scanning direction of the glass substrate 1.

In this recrystallization, laser beams are converted into linear beams elongated in the Y direction using a beam expander.

The laser irradiation intensities in the X direction and the Y direction during such an operation are shown in Fig. 12 and Fig. 13. In Fig. 12 and Fig. 13, an axis of abscissas indicates the position and an axis of ordinates indicates the laser beam intensity.

The laser beam intensity distribution in the X direction exhibits the substantially Gauss distribution, while the laser beam intensity distribution in the Y direction generates a slight difference in intensity within a crystallization range between

Y1-Y2 (a range indicated by C shown in Fig. 13), and the state of crystallization is changed in response to the difference in intensity.

Further, even when the distribution of intensity of laser beam at the position in the Y direction is fixed, there arises a following drawback.

That is, in view of the fact that it is difficult to continue the growth of crystals in the lateral direction over an extremely long region, there exists the following case. That is, in the course of the formation of the pseudo single crystal region 3, the irradiation of the laser beams 4 to the polycrystalline silicon film 2 is prevented or the intensity of the laser beams 4 is decreased so as to stop the growth of the crystals in the lateral direction temporarily. Then, at the position away from one pseudo single crystal region 3 which is already formed, the laser beams having a given intensity is again irradiated to form another pseudo single crystal region 3 at another position separate from the previous position.

Further, although the laser beams 4 have a shape which is elongated in the direction (Y direction) which crosses the scanning direction (X direction) rather than the scanning direction, a length in the Y direction is extremely small compared to the size of the substrate such as the glass substrate 1. Accordingly, there may be a case that by performing the reciprocating scanning while shifting the position in the Y

direction each time the scanning reaches an end of the glass substrate 1, another pseudo single crystal region 3 is formed at a position different from the previous position.

In this manner, when the pseudo single crystal regions 3 are formed at a plurality of positions in two or more times separately, there may be a case that the state of the crystallization differs delicately for every formed pseudo single crystal region 3 or a case that the characteristics of the thin film transistor formed on the pseudo single crystal region 3 differs for every pseudo single crystal region 3.

By forming the thin film transistor on the semiconductor layer formed by the method described in the above-mentioned non-patent literature 1, it is possible to prepare a liquid crystal display module which incorporates peripheral circuits such as drive circuits therein.

In such a liquid crystal display module which incorporates the peripheral circuits therein, a reference voltage generating circuit for a digital/analogue converting circuit (DAC) incorporated in the liquid crystal display module is necessary or a differential amplifying circuit is necessary for buffer amplifiers which are provided to respective drain signal lines.

The differential amplifying circuit requires a pair of transistors which agree in transistor characteristics (or having a small relative error in transistor characteristics thus having a favorable matching).

However, as mentioned previously, in the above-mentioned non-patent literature 1, depending on the intensity distribution of laser beams for recrystallization, the pair of transistors delicately differ in a crystallized state and hence, there arises a drawback that the relative error in the characteristics of the pair of transistors which are formed on the recystallized silicon layer is increased.

Accordingly, there has been a case that the thin film transistor which is formed on the semiconductor layer by the method described in the previously-mentioned non-patent literature 1 gives rise to a problem when the transistor is applied to an analogue circuit which is required to have high accuracy such as a buffer amplifier for a drain driver which is required to exhibit an offset voltage of several mV or the like.

Further, the occurrence of drawbacks explained heretofore is not limited to the pseudo single crystallization technique described in the non-patent literature 1 and the drawbacks may arise in a case that the pseudo single crystal region 3 which grows the elongated strip-like crystals in the lateral direction is formed using other similar pseudo single crystallization technique.

This is because these cases are common with respect to irregularities of the intensity distribution of the laser beams 4 in the direction (Y direction) which intersects the scanning

direction (X direction) or the irregularities of the crystallized state when the separated pseudo single crystal regions 3 are formed at the plurality of positions.

The drawbacks attributed to such causes are hardly apparent when the particle size of the polycrystal is small since the irregularities of the characteristics are made uniform due to the presence of a large number of polycrystals in respective thin film transistors. However, when the elongated strip-like crystals are grown in the lateral direction, the number of the crystals present in respective thin film transistors becomes small and hence, the irregularities become apparent.

The present invention has been made to overcome the above-mentioned drawbacks of the related art and an advantage of the present invention is to provide a display device which is capable of reducing the irregularities of characteristics of pair of transistors which are transistors formed by a pseudo single crystallizing technique and are used in a differential amplifying circuit or the like.

The above-mentioned and other advantages and novel features of the present invention will become apparent from the description of this specification and attached drawing.

To briefly explain the summary of the representative inventions out of the inventions disclosed in this specification, they are as follows.

The present invention is directed to a display device which includes a semiconductor layer formed on a substrate and a plurality of thin film transistors having semiconductor layers, wherein semiconductor layer includes a first pseudo single crystal region and a second pseudo single crystal region which is formed at a position separated from the first pseudo single crystal region, and out of the plurality of thin film transistors, two or more thin film transistors which are required to exhibit small irregularities relative to each other as the characteristics of the transistors are arranged in the same pseudo single crystal region.

Further, the present invention is also directed to a display device which includes semiconductor layers formed on a substrate and having pseudo single crystal regions and a plurality of thin film transistors arranged in the inside of the pseudo single crystal regions, wherein in the pseudo single crystal region, the semiconductor includes crystals which are grown in an elongate strip-like shape in the direction parallel to the substrate, and out of the plurality of thin film transistors, two or more thin film transistors which are required to exhibit small irregularities relative to each other as the characteristics of the transistors have the direction of a length of gates of the respective thin film transistors arranged with an inclination of within ±20 degree with respect to the longitudinal direction of the strip-like grown crystals and

are arranged such that when channel regions of the respective thin film transistors are imaginarily extended in parallel to the growth direction of the strip-like grown crystals, at least portions of the channel regions superpose each other.

Further, in the present invention, a rate of the superposition is 50% or more, and preferably 80% or more.

Further, the present invention is directed to a display device which includes semiconductor layers formed on a substrate and having pseudo single crystal regions and a plurality of thin film transistors arranged in the inside of the pseudo single crystal regions, wherein in the pseudo single crystal region, the semiconductor includes crystals which are grown in an elongate strip-like shape in the direction parallel to the substrate, and out of the plurality of thin film transistors, two or more thin film transistors which are required to exhibit small irregularities relative to each other as the characteristics of the transistors have the direction of a length of gates of the respective thin film transistors arranged with an inclination of within ±20 degree with respect to the longitudinal direction of the strip-like grown crystals and are arranged such that the directions of currents which flow in the respective thin film transistors are aligned with each other.

Here, two or more thin film transistors which are required to exhibit small irregularities relative to each other as the

characteristics of the transistors are formed of a differential pair of transistors which constitute a differential amplifying circuit, a pair of transistors of an active load circuit which constitute a differential amplifying circuit, or a pair of transistors of an active load circuit which constitute a differential amplifying circuit and a transistor having a gate thereof to which an output voltage of the active load circuit is applied.

Further, two or more thin film transistors which are required to exhibit small irregularities relative to each other as the characteristics of the transistors are formed of a pair of transistors which constitute a current mirror circuit or a plurality of transistors which are connected in parallel to each other and equivalently constitute one transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the schematic constitution of a liquid crystal display device of an embodiment of the present invention;

Fig. 2 is a schematic view for explaining a pseudo single crystal region in the liquid crystal display device of the embodiment of the present invention;

Fig. 3 is a structural view which schematically showing a thin film transistor formed in the pseudo single crystal region;

Fig. 4 is a schematic view for explaining an arranging method of the thin film transistor in the embodiment of the present invention;

Fig. 5 is a schematic view for explaining an arranging method of the thin film transistor in the embodiment of the present invention;

Fig. 6 is a schematic view for explaining another example of an arranging method of the thin film transistor in the embodiment of the present invention;

Fig. 7 is a circuit diagram showing a differential amplifying circuit to which the arranging method of the thin film transistor in the embodiment of the present invention is applied;

Fig. 8 is a view showing a first layout example of the differential amplifying circuit shown in Fig. 7;

Fig. 9 is a view showing a second layout example of the differential amplifying circuit shown in Fig. 7;

Fig. 10 is a view showing a third layout example of the differential amplifying circuit shown in Fig. 7;

Fig. 11 is a view for explaining a pseudo single crystallizing method of polycrystal silicon using a laser.

Fig. 12 is a graph showing the intensity of laser beam irradiation in the X direction in the pseudo single crystallizing method of polycrystal silicon shown in Fig. 11.

Fig. 13 is a graph showing the intensity of laser beam

irradiation in the Y direction in the pseudo single crystallizing method of polycrystal silicon shown in Fig. 11.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention are explained in detail in conjunction with drawings.

Here, in all drawings which are served for explaining the embodiments, parts to which the same functions are given are indicated by same symbols and their repeated explanation is omitted.

Fig. 1 is a block diagram showing the schematic constitution of a liquid crystal display device of the embodiment of the present invention. The liquid crystal display device of this embodiment includes a semiconductor layer prepared by the previously-mentioned pseudo single crystallizing technique (for example, SELAX).

The liquid crystal display device of this embodiment includes a drain driver 100, a timing control circuit 200, a reference data generating circuit 300, a ramp voltage generating circuit 400, a gate driver 500 and a display part 800.

In the display part 800, a plurality of pixels which are arranged in a matrix array, drain signal lines D which supply a video signal voltage to respective pixels, and gate signal lines G which supply a scanning signal voltage to the respective pixels are formed.

Each pixel includes a pixel transistor (GTFT) which is constituted of a thin film transistor and the pixel transistor (GTFT) is connected between a drain signal line D and a pixel electrode (ITO1), and a gate thereof is connected to a gate signal line G.

Between the pixel electrode (ITO1) and a counter electrode (also referred to as "common electrode" not shown in the drawing), liquid crystal is sealed and hence, a pixel capacity (CLC) is equivalently connected between the pixel electrode (ITO1) and the counter electrode.

Here, in Fig. 1, for the sake of brevity of the illustration, only one thin film transistor (GTFT) is shown.

The drain driver 100 is constituted of a shift register 110, a latch circuit 120, a latch circuit 130, a comparator 140 and a sample holding circuit 150.

The timing control circuit 200 receives a clock (CLK), a horizontal synchronous signal (Hs), a vertical synchronous signal (Vs), a display timing signal (DTMG) and display data (Di) as input signals and generates signals which control the drain driver 100, the reference data generating circuit 300, the ramp voltage generating circuit 400 and the gate driver 500.

Hereinafter, the driving method of the liquid crystal display device of this embodiment is explained.

In general, for preventing the degradation of the liquid

crystal, a liquid crystal display device adopts an alternating driving method. In the liquid crystal display device of this embodiment, as the alternating driving method, a dot inversion method is adopted.

This dot inversion method is a driving method in which video signals which are applied to the pixels which are arranged close to each other assume polarities opposite to each other in the row direction as well as in the column direction.

The shift register 110 is operated in response to a start signal (HST) and a clock signal (HCK) transmitted from the timing control circuit 200 and outputs a multi-phase pulse which controls the latch circuit 120.

The latch circuit 120, in response to this multi-phase pulse, sequentially holds the display data (DATA) transmitted from the timing control circuit 200 one after another for one horizontal scanning line.

Upon receiving inputting of a timing signal (LT) which is indicative of the completion of transfer of display data for one horizontal scanning line transmitted from the timing control circuit 200, the latch circuit 130 simultaneously holds the display data of the latch circuit 120 at the same timing.

The comparator 140 compares a quantity of display data held by the latch circuit 130 and a quantity of the reference data (NCNT) which are transmitted from the reference data generating circuit 300.

To be more specific, the comparator 140 is initialized in response to an initializing signal (RS) transmitted from the timing control circuit 200 and, thereafter, outputs a High level (hereinafter referred to as "H level") when the reference data (NCNT) is smaller than the display data or equal to the display data.

The reference data generating circuit 300 is an up counter which receives the clock (CK) and the initializing signal (RS) transmitted from the timing control circuit 200 as inputs.

The sample holding circuit 150 receives an output of the comparator 140, the alternating signals (M, MB), outputs (RAMP1, RAMP2) of the ramp voltage generating circuit 400 as inputs and outputs a pixel drive voltage to the drain signal lines D on the display part 800.

Here, the alternating signal (M) and the alternating signal (MB) are logic signals which control the polarity of the video signal voltage applied to the pixel electrode of the display part 800 and have the relationship of inversion and hence, their logics are inverted for every line or for every frame.

The output (RAMP1) of the ramp voltage generating circuit 400 is a ramp voltage of positive polarity and the output (RAMP2) of the ramp voltage generating circuit 400 is a ramp voltage of negative polarity. With respect to respective ramp voltages of the output (RAMP1) and the output (RAMP2), their absolute

values of inclination are set equal to each other.

The sample holding circuit 150 includes a buffer amplifier (BAA) which amplifies the ramp voltage (RAMP1) of positive polarity and a buffer amplifier (BAB) which amplifies the ramp voltage (RAMP2) of negative polarity.

In this embodiment, the drain signal lines D are driven by the buffer amplifiers and hence, the fluctuation of load of the ramp voltage generating circuit 400 attributed to the display images can be suppressed whereby it is possible to display images of high quality.

Here, the buffer amplifier (BAA) and the buffer amplifier (BAB) are provided for every two neighboring drain signal lines (for example, the drain signal line (D1) and the drain signal line (D2) shown in Fig. 1), wherein two drain signal lines use the buffer amplifier (BAA) and the buffer amplifier (BAB) in common.

Accordingly, in this embodiment, to the sample holding circuit 150, outputs of two comparators 140 which correspond to two neighboring drain signal lines are inputted.

Then, due to the operation of switching elements (SW1) which are controlled in response to the alternating signals (M, MB), an output of one comparator 140 is outputted to a switching element (SWA) which samples the ramp voltage (RAMP1) of positive polarity or a switching element (SWB) which samples the ramp voltage (RAMP2) of negative polarity. Simultaneously,

an output of another comparator 140 is outputted to the switching element (SWB) or the switching element (SWA).

Further, due to the operation of switching elements (SW2) which are controlled in response to the alternating signals (M, MB), an output of the buffer amplifier (BAA) which amplifies the ramp voltage (RAMP1) of positive polarity is outputted to one drain signal line or another drain signal line and, at the same time, an output of the buffer amplifier (BAB) which amplifies the ramp voltage (RAMP2) of negative polarity is outputted to another drain signal line or one drain signal line.

For example, with respect to the case shown in Fig. 1, when the alternating signal (M) assumes H level and the alternating signal (MB) assumes L level, the output of the comparator 140 corresponding to the drain signal line (D1) is inputted to the switching element (SWA) and the output of the comparator 140 corresponding to the drain signal line (D2) is inputted to the switching element (SWB). Further, the output voltage of the buffer amplifier (BAA) is inputted to the drain signal line (D1) and the output voltage of the buffer amplifier (BAB) is inputted to the drain signal line (D2).

Further, when the alternating signal (M) assumes L level and the alternating signal (MB) assumes H level, the output of the comparator 140 corresponding to the drain signal line (D1) is inputted to the switching element (SWB) and the output of the comparator 140 corresponding to the drain signal line

(D2) is inputted to the switching element (SWA). Further, the output voltage of the buffer amplifier (BAB) is inputted to the drain signal line (D1) and the output voltage of the buffer amplifier (BAA) is inputted to the drain signal line (D2).

Accordingly, the polarity of the video signal supplied to the drain signal lines D can be inverted for every horizontal scanning line between the neighboring drain signal lines. In Fig. 1, symbol LS indicates a level shift circuit.

The gate driver 500 is operated in response to the start signal (VST) and the clock (CL) transmitted from the timing control circuit 200 and outputs the scanning signal which sequentially turns on the pixel transistors (GTFT) one after another for one horizontal scanning line period to the gate signal lines G on the display part 800.

Images are displayed on the display part 800 in accordance with such operations.

In this embodiment, since the alternating is performed by the sample holding circuit 150, the ramp voltages (RAMP1, RAMP2) which are outputted from the ramp voltage generating circuit 400 can be held at the positive polarity and the negative polarity without changing the polarity whereby the voltage amplitude can be decreased and the power consumption can be reduced.

Further, the output impedance of the ramp generating circuit 400 can be reduced and hence, the delay time can be

shortened whereby the display images of high quality can be obtained.

Fig. 2 is a schematic view for explaining the pseudo single crystal regions in the liquid crystal display device of this embodiment.

As shown in Fig. 2, in this embodiment, a peripheral circuit 810 is arranged around a periphery of the display part 800 and the drain driver 100, the timing control circuit 200, the reference data generating circuit 300, the ramp voltage generating circuit 400 and the gate driver 500 are arranged in the peripheral circuit 810.

These circuits are formed of semiconductor layers (above-mentioned pseudo single crystal regions) which are formed on the glass substrate 1.

Here, the above-mentioned pseudo single crystal regions 820 (corresponding to the symbol 3 in Fig. 11) are formed in an island shape in an arrow (→) direction shown in Fig. 2. This is because the pseudo single crystal regions 820 are formed by scanning the glass substrate 1 in the direction opposite to the arrow (→) direction shown in Fig. 2. A plurality of thin film transistors are arranged in one pseudo single crystal region 820.

As mentioned previously, when the polycrystal silicon is melt and recrystallized to form the pseudo single crystal region, the state of the recrystallization is changed depending

on the difference in the intensity of the laser beam irradiation.

Accordingly, when the thin film transistors are formed on the pseudo single crystal region 820, there arise the irregularities in the characteristics (for example, mobility or the like) of the thin film transistors for every pseudo single crystal region 820.

Accordingly, in this embodiment, a plurality of thin film transistors which are required to have small irregularities as the characteristics of the thin film transistors are formed within the same pseudo single crystal region.

That is, for example, a differential pair of transistors of a differential amplifying circuit or a pair of transistors which constitute a current mirror circuit or the like are formed on the same pseudo single crystal region. Due to such a constitution, it is possible to reduce the irregularities of characteristics of the thin film transistors.

Fig. 3 is a structural view which schematically shows the thin film transistors formed in the pseudo single crystal region.

The thin film transistor shown in Fig. 3 is formed such that the pseudo single crystal region 820 is formed into a smaller island-like region 5 by etching or the like, a gate oxide film 13 is formed on the region 5, and a gate electrode 12 is formed on the gate oxide film 13. A plurality of regions 5 are formed in one pseudo single crystal region 820 and hence, a plurality

of thin film transistors are formed in one pseudo single crystal region 820.

Here, in Fig. 3, numeral 10 indicates a source region, numeral 11 indicates a drain region, an arrow A indicates the scanning direction of the glass substrate 1, and an arrow B indicates the crystallization direction.

With respect to the thin film transistors which are formed on the pseudo single crystal region 820 formed in an island shape, to obtain the favorable mobility, it has been known to arrange the direction of the source-drain (direction of a length of a gate) substantially parallel to the crystal growth direction (direction of the arrow B in Fig. 3). In this case, the thin film transistors may be arranged such that the direction of the length of the gate makes an inclination within ±20 degrees with respect to the longitudinal direction of the crystals.

Hereinafter, the arranging method of a plurality of thin film transistors which are required to have small irregularities as the characteristics of the thin film transistors of this embodiment is explained by taking a pair of thin film transistors as an example.

Fig. 4 is a schematic view for explaining the arranging method of thin film transistors according to this embodiment.

As shown in Fig. 4, in this embodiment, not only the source-drain direction of respective thin film transistors (TFT1, TFT2) are arranged substantially parallel (within ±20

degrees) to the crystal growth direction (direction of the arrow B shown in Fig. 4) but also a straight line which connects the centers of gate widths (W) of the respective thin film transistors (TFT1, TFT2) is arranged parallel to the crystal growth direction.

By adopting such an arrangement, in the portion of the pseudo single crystal region which is melt with the same laser beam intensity irradiation and thereafter recrystallized, the pair transistors (TFT1, TFT2) are formed and hence, it is possible to obtain the favorable matching of the transistor characteristics by reducing the irregularities of the characteristics of the thin film transistors.

Here, in this embodiment, it is not always necessary to arrange the straight line which connects the centers of the gate widths (W) of the respective thin film transistors (TFT1, TFT2) parallel to the crystal growth direction.

As shown in Fig. 5, two or more thin film transistors (TFT1, TFT2) which are required to have small irregularities as the characteristics of the thin film transistors are arranged such that the direction of the length of the gates of the respective thin film transistors makes an inclination within ±20 degrees with respect to the longitudinal direction of the crystals which are grown in a strip shape. At the same time, these thin film transistors (TFT1, TFT2) may be also arranged such that a region which is formed by imaginarily extending

the channel region of the thin film transistor (TFT1) having the gate width (E) in parallel to the growth direction of the strip-like grown crystal and a region which is formed by imaginarily extending the channel region of the thin film transistor (TFT2) having the gate width (W) in parallel to the growth direction of the strip-like grown crystal have at least portions thereof superposed each other.

Here, a rate of such superposed portions is 50% or more, and preferably 80% or more. That is, it is desirable that the length of D shown in Fig. 5 is 50% or more, and preferably 80% or more of the gate width (W) of the thin film transistor (TFT2).

Here, in addition to the above-mentioned embodiment, it is further desirable that these thin film transistors (TFT1, TFT2) are arranged in the inside of the same pseudo single crystal region 820 out of the plurality of pseudo single crystal regions 820. The same goes for the embodiments explained hereinafter.

Fig. 6 is a schematic view for explaining another example of the arranging method of thin film transistors of this embodiment.

The example shown in Fig. 6 is directed to the arranging method in which the irregularities of the characteristics of two thin film transistors (TFT1, TFT2) which differ in the gate width (W1, W2) can be decreased.

Also in this embodiment, not only the source-drain

direction is set substantially parallel to the crystal growth direction (arrow direction B shown in Fig. 6), but also a straight line which connects the centers of the gate widths (W1, W2) is arranged parallel to the crystal growth direction.

This example is particularly effective when the gate width is sufficiently smaller than a long side of the laser beams. This is because the distribution of laser beam intensity substantially approximates a straight line in the narrow width region and hence, the correlation between the characteristics of the thin film transistor and the crystallized state at the center of the gate width can be established.

Fig. 7 is a circuit diagram showing a differential amplifying circuit to which the arranging method of the thin film transistors of this embodiment is applied.

In Fig. 7, N-type MOS transistors (simply referred to as NMOS hereinafter) (431, 432) are differential-pair thin film transistors which constitute a differential pair. Further, P-type MOS transistors (simply referred to as PMOS hereinafter) (433, 434) are a pair of thin film transistors which constitute an active load circuit and PMOS435 is a transistor having a gate to which an output of the active load circuit is applied.

Further, the NMOS (437, 438) or the NMOS (437, 439) are a pair of thin film transistors which constitute the current mirror circuit respectively.

Fig. 8 is a view showing a first example of layout of

the differential amplifying circuit show in Fig. 7.

Portions surrounded by an ellipse 30 shown in Fig. 8 are regions in which the PMOS(433, 434, 435) shown in Fig. 7 are arranged, wherein respective thin film transistors are arranged such that a line which connects the centers of the gate widths of respective thin film transistors is substantially arranged parallel to the crystallizing direction.

Further, a portion surrounded by an ellipse 31 shown in Fig. 8 is a region in which the NMOS(431, 432) shown in Fig. 7 are arranged, wherein respective thin film transistors are arranged such that a line which connects the centers of the gate widths of respective thin film transistors is substantially arranged parallel to the crystallizing direction.

In the same manner, a portion surrounded by an ellipse 32 shown in Fig. 8 is a region in which the NMOS(437 to 439) shown in Fig. 7 are arranged, wherein respective thin film transistors are arranged such that a line which connects the centers of the gate widths of respective thin film transistors is substantially arranged parallel to the crystallizing direction.

Here, the PMOS 435 and the NMOS 439 have a gate width thereof set to a value twice as large as the gate width of other transistors. Further, all thin film transistors shown in Fig. 8 are arranged in the inside of the same pseudo single crystal region 820.

Fig. 9 is a view showing a second example of layout of the differential amplifying circuit show in Fig. 7.

A portion which makes this example differs from the example shown in Fig. 8 lies in the layout method of the PMOS 435 and the NMOS 439.

In the example shown in Fig. 9, two transistors having the same gate width as the width of another transistor are used so as to increase a current (source-drain current) capacity twice.

Fig. 10 is a view showing a third example of layout of the differential amplifying circuit show in Fig. 7.

A portion which makes this example differ from the example shown in Fig. 8 lies in that the directions of currents which flow in respective transistors (source-drain currents "i" shown in Fig. 10) are aligned with each other. Due to such a layout, it is possible to decrease the irregularities of the characteristics of the thin film transistors and hence, matching property of a transistor pair which constitute a pair can be enhanced.

Here, in Fig. 8 to Fig. 10, × indicates through holes (contact holes) while a dotted line indicates a wiring layer formed as a lower layer.

As explained above, in this embodiment, a plurality of thin film transistors which are required to have small irregularities as the characteristics of the thin film

transistors, for example, a pair of transistors, are arranged such that the gate widths of the pair transistors are set equal and, at the same time, the straight line which connects the centers of the gate widths become parallel to the crystallizing direction of the pseudo single crystal region.

As a result, the distribution of intensity of laser beams irradiated to the channel regions of the pair transistors becomes equal and hence, the relative error in the characteristics of the pair transistors can be decreased.

Further, even when the matching of transistors which differ in the gate width is acquired using the current mirror circuit, the pair transistors are arranged such that the straight line which connects the centers of the gate widths becomes parallel to the crystallizing direction.

As a result, the average value of the intensity of laser beams in the gate width direction can be made equal and hence, the relative error in the characteristics of the pair transistors can be decreased.

Further, when the current ratio of integer times is ensured by the current mirror circuit, for example, using the transistor having the gate width which is equal to the reference width and the transistors having the same gate width which are integer times larger than the former transistor in number, all of these transistors are arranged such that the straight line which connects the centers of the gate widths becomes parallel to

the crystallizing direction.

As a result, the distribution of intensity of laser beams irradiated to the channel regions of the pair transistors becomes equal and hence, the relative error in the characteristics of the pair transistors can be decreased.

Here, it is possible to combine these embodiments with modifications which are explained in conjunction with Fig. 5.

Due to such constitutions, according to the display device of this embodiment, since the reference voltage generating circuit which supplies the reference voltage to the built-in DAC can be formed on the substrate on which the display part 800 is also formed, it is possible to reduce the exteriorly mounted parts whereby it is possible to provide the highly reliable display device.

Further, since the buffer amplifiers of the drain driver can be formed on the substrate on which the display part 800 is formed, it is possible to provide the display of high quality image by a line sequential driving method.

Here, although the present invention is explained in conjunction with the embodiments which are applied to the liquid crystal display module, it is needless to say that the present invention is not limited to these embodiments and the present invention is applicable to other display devices such as the EL display device.

Although the inventions which are made by the inventors

are specifically explained based on the above-mentioned embodiments, it is needless to say that the present inventions are not limited to these embodiments and various modifications are conceivable without departing from the gist of the present inventions.

To briefly explain the advantageous effect obtained by the typical inventions out of the inventions disclosed in this specification, it is as follows.

According to the display device of the present invention, it is possible to reduce the irregularities of characteristics of the pair transistors which are formed using the pseudo single crystallizing technique and are used in the differential amplifying circuit or the like.